REMARKS

This paper is responsive to the Non-Final Office Action mailed on September 6, 2006. Claims 1-20 were examined and rejected to. Applicant thanks the Examiner for a detailed and thoughtful examination of all the claims.

Claims 1, 3-11, 13-15, and 17-20 remain in this application for further examination, wherein claims 1, 11, 13, 15, 19, and 20 are currently amended. Original claims 2, 12, and 16 are canceled.

Claim Rejections – 35 U.S.C. §102(b)

Claims 1-20 stand rejected under 35 U.S.C. §102(b) as being anticipated by one of Schenkel et al. (US 6,518,733) and Hall et al. (US 6,597,221). This rejection is respectfully traversed.

As to claims 1 and 3-10:

The independent claim 1 is currently amended by incorporating all of the limitations of claim 2 as follows:

> *"a first current detector for detecting the primary winding current to generate a primary current detection signal;*
>
> *a reference voltage generator controlled by the soft-start circuit to generate a soft-start reference voltage; and*
>
> *a first voltage comparator for comparing the primary current detection signal with the soft-start reference voltage so as to output an ON-time ending signal to the switch controller"*

According to the currently amended claim 1, the soft-start reference voltage is compared at the first voltage comparator with the primary current detection signal, which is generated by the first current detector as a representative of the primary winding current. Because none of Schenkel et al. (US 6,518,733) and Hall et al. (US 6,597,221) discloses

or suggests such limitations, the independent claim 1 is thus believed to be allowable over the art of record, and all claims dependent therefrom are likewise believed to be allowable at least for this reason.

It is obvious that Schenkel et al. (US 6,518,733) fails to disclose or suggest any circuitry or function relating to any possible kind of soft-start operation. Although Hall et al. (US 6,597,221) specifically discloses the soft-start circuit (62), the duty cycle control signal (DUTY CYCLE), and the soft-start mode of operation (see column 8, line 9 to column 10, line 49), the prior art is completely different from the Applicant's claimed soft-start circuitry, function, or operation. Referring to FIG. 2 of Hall et al. (US 6,597,221), signal DUTY CYCLE is generated by the soft-start circuit (62) for modifying the duty cycle of signal GATE, particularly for gradually increasing the duty cycle of signal GATE from the predetermined minimum duty cycle towards a predetermined maximum duty cycle (see column 4, lines 41-52). **To achieve the prior art soft-start mode of operation, signal DUTY CYCLE is compared at the comparator (84) with signal RAMP generated by the oscillator (83) of the pulse width modulator (PWM) (75). It should be noted that signal RAMP is a sawtooth waveform having a fixed frequency (see column 6, lines 60-61), which has nothing to do with the primary winding current.** Therefore, Hall et al. (US 6,597,221) fails to disclose or suggest at least: (1) a first current detector for detecting the primary winding current to generate a primary current detection signal, and/or (2) a first voltage comparator for comparing the primary current detection signal with the soft-start reference voltage so as to output an ON-time ending signal to the switch controller.

As to claims 11, 13, and 14:

The independent claim 11 is currently amended by incorporating all of the limitations of claim 12 as follows:

"a first current detector for detecting the primary winding current to generate a primary current detection signal;

a reference voltage generator for generating a soft-start reference voltage; and

a first voltage comparator for comparing the primary current detection signal with the soft-start reference voltage so as to output an ON-time ending signal to the switch controller"

According to the currently amended claim 11, the soft-start reference voltage is compared at the first voltage comparator with the primary current detection signal, which is generated by the first current detector as a representative of the primary winding current. Because none of Schenkel et al. (US 6,518,733) and Hall et al. (US 6,597,221) discloses or suggests such limitations, the independent claim 11 is thus believed to be allowable over the art of record, and all claims dependent therefrom are likewise believed to be allowable at least for this reason.

It is obvious that Schenkel et al. (US 6,518,733) fails to disclose or suggest any circuitry or function relating to any possible kind of soft-start operation. Although Hall et al. (US 6,597,221) specifically discloses the soft-start circuit (62), the duty cycle control signal (DUTY CYCLE), and the soft-start mode of operation (see column 8, line 9 to column 10, line 49), the prior art is completely different from the Applicant's claimed soft-start circuitry, function, or operation. Referring to FIG. 2 of Hall et al. (US 6,597,221), signal DUTY CYCLE is generated by the soft-start circuit (62) for modifying the duty cycle of signal GATE, particularly for gradually increasing the duty cycle of signal GATE from the predetermined minimum duty cycle towards a predetermined maximum duty cycle (see column 4, lines 41-52). **To achieve the prior art soft-start mode of operation, signal DUTY CYCLE is compared at the comparator (84) with signal RAMP generated by the oscillator (83) of the pulse width modulator (PWM) (75). It should be noted that signal RAMP is a sawtooth waveform having a fixed frequency (see column 6, lines 60-61), which has nothing to do with the primary winding current.** Therefore, Hall et al. (US 6,597,221) fails to disclose or suggest at

least: (1) a first current detector for detecting the primary winding current to generate a primary current detection signal, and/or (2) a first voltage comparator for comparing the primary current detection signal with the soft-start reference voltage so as to output an ON-time ending signal to the switch controller.

As to claims 15, 17, and 18:

The independent claim 15 is currently amended by incorporating all of the limitations of claim 16 as follows:

> *"a first current detector for detecting the primary winding current to generate a primary current detection signal;*
>
> *a reference voltage generator for generating a soft-start reference voltage; and*
>
> *a first voltage comparator for comparing the primary current detection signal with the soft-start reference voltage so as to output an ON-time ending signal to the switch controller"*

According to the currently amended claim 15, the soft-start reference voltage is compared at the first voltage comparator with the primary current detection signal, which is generated by the first current detector as a representative of the primary winding current. Because none of Schenkel et al. (US 6,518,733) and Hall et al. (US 6,597,221) discloses or suggests such limitations, the independent claim 15 is thus believed to be allowable over the art of record, and all claims dependent therefrom are likewise believed to be allowable at least for this reason.

It is obvious that Schenkel et al. (US 6,518,733) fails to disclose or suggest any circuitry or function relating to any possible kind of soft-start operation. Although Hall et al. (US 6,597,221) specifically discloses the soft-start circuit (62), the duty cycle control signal (DUTY CYCLE), and the soft-start mode of operation (see column 8, line 9 to column 10, line 49), the prior art is completely different from the Applicant's claimed

soft-start circuitry, function, or operation. Referring to FIG. 2 of Hall et al. (US 6,597,221), signal DUTY CYCLE is generated by the soft-start circuit (62) for modifying the duty cycle of signal GATE, particularly for gradually increasing the duty cycle of signal GATE from the predetermined minimum duty cycle towards a predetermined maximum duty cycle (see column 4, lines 41-52). **To achieve the prior art soft-start mode of operation, signal DUTY CYCLE is compared at the comparator (84) with signal RAMP generated by the oscillator (83) of the pulse width modulator (PWM) (75). It should be noted that signal RAMP is a sawtooth waveform having a fixed frequency (see column 6, lines 60-61), which has nothing to do with the primary winding current.** Therefore, Hall et al. (US 6,597,221) fails to disclose or suggest at least: (1) a first current detector for detecting the primary winding current to generate a primary current detection signal, and/or (2) a first voltage comparator for comparing the primary current detection signal with the soft-start reference voltage so as to output an ON-time ending signal to the switch controller.

As to claims 19 and 20:

The independent claim 19 is currently amended by incorporating some of the limitations of claim 20 as follows:

> *"a first current detector for detecting the primary winding current to generate a primary current detection signal;*
>
> *a reference voltage generator for generating a soft-start reference voltage; and*
>
> *a first voltage comparator for comparing the primary current detection signal with the soft-start reference voltage so as to output an ON-time ending signal to the switch controller"*

According to the currently amended claim 19, the soft-start reference voltage is compared at the first voltage comparator with the primary current detection signal, which is

generated by the first current detector as a representative of the primary winding current. Because none of Schenkel et al. (US 6,518,733) and Hall et al. (US 6,597,221) discloses or suggests such limitations, the independent claim 19 is thus believed to be allowable over the art of record, and all claims dependent therefrom are likewise believed to be allowable at least for this reason.

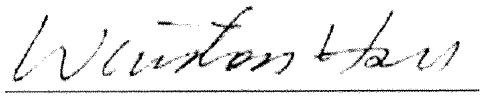
It is obvious that Schenkel et al. (US 6,518,733) fails to disclose or suggest any circuitry or function relating to any possible kind of soft-start operation. Although Hall et al. (US 6,597,221) specifically discloses the soft-start circuit (62), the duty cycle control signal (DUTY CYCLE), and the soft-start mode of operation (see column 8, line 9 to column 10, line 49), the prior art is completely different from the Applicant's claimed soft-start circuitry, function, or operation. Referring to FIG. 2 of Hall et al. (US 6,597,221), signal DUTY CYCLE is generated by the soft-start circuit (62) for modifying the duty cycle of signal GATE, particularly for gradually increasing the duty cycle of signal GATE from the predetermined minimum duty cycle towards a predetermined maximum duty cycle (see column 4, lines 41-52). **To achieve the prior art soft-start mode of operation, signal DUTY CYCLE is compared at the comparator (84) with signal RAMP generated by the oscillator (83) of the pulse width modulator (PWM) (75). It should be noted that signal RAMP is a sawtooth waveform having a fixed frequency (see column 6, lines 60-61), which has nothing to do with the primary winding current.** Therefore, Hall et al. (US 6,597,221) fails to disclose or suggest at least: (1) a first current detector for detecting the primary winding current to generate a primary current detection signal, and/or (2) a first voltage comparator for comparing the primary current detection signal with the soft-start reference voltage so as to output an ON-time ending signal to the switch controller.

Summary

In summary, claims 1, 3-11, 13-15, and 17-20 remain in this application for further examination. Through the amendments by further including limitations with respect to

the control circuit, all of the remaining claims are believed to be allowable over the art of record, and a Notice of Allowance to that effect is respectfully solicited.

Sincerely yours,



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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 13 hours behind the Taiwan time, i.e. 9 AM in D.C. = 10 PM in Taiwan.)